REMARKS

Upon entry of this response, claims 1-3, 5-12, 9-12 and 24-26 remain pending. Reconsideration and allowance of the pending claims are respectfully requested.

Indication of Allowed Subject Matter

Applicant appreciates the allowance of claims 9-12.

Rejections under 35 U.S.C. 102(b)

The Office Action indicates that claims 1, 5, 8 and 24 stand rejected under 35 U.S.C. 102(e) as allegedly anticipated by Blish et al. (U.S. 6,362,524). Applicants respectfully traverse the rejection.

In this regard, claim 1 recites:

> 1. A method of fabricating an integrated circuit seal ring comprising:
> providing an active area including semiconductor device structures; and
> forming a continuous conductive loop around the perimeter of said integrated circuit wherein said conductive loop has ***a plurality of sections having at least two different alternating widths wherein each of said sections has a different width from its adjacent sections*** wherein characteristic impedance of each of said two different widths is different, wherein said conductive loop forms said seal ring.

(*Emphasis Added*).

Applicant respectfully asserts that *Blish* is legally deficient for the purpose of anticipating claim 1, because at least the features/limitations emphasized above in claim 1 are not taught by *Blish*. For example, *Blish* does not teach that each of said sections has a different width from its adjacent sections. Specifically, all the sections in *Blish* (legs 122) are of similar width and length (see column 4, lines 36-37, and FIG. 12).

In addition, Applicant respectfully asserts that claim 1 appears to have been misinterpreted. In section 6, the Office Action indicates that FIG. 12 of *Blish* discloses that the protruding portions are wider than their adjacent portions. However, the term "width" has been used in accordance with its common and ordinary meaning, i.e. "width" means *across* the conductive loop. In contrast, the Office Action appears to be referring to the length of the section of *Blish* for rejecting claim 1. Applicant respectfully asserts that this is an improper use of *Blish* because "length" means *along* the conductive loop. Thus, Applicant asserts that the rejection is improper and should be removed.

With respect to claim 5, that claim recites:

> 5. A method of fabricating an integrated circuit seal ring comprising:
> providing an active area including semiconductor device structures; and
> forming a continuous conductive loop around the perimeter of said integrated circuit ***by patterning and forming a plurality of stacked, interconnected, conductive layers wherein said conductive loop has a plurality of sections having at least two different alternating widths***, wherein said conductive loop forms said seal ring.

(*Emphasis Added*).

Applicant respectfully asserts that *Blish* is legally deficient for the purpose of anticipating claim 5, because at least the features/limitations emphasized above in claim 5 are not taught by *Blish*. For example, *Blish* does not teach or suggest forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers. Specifically, the sections 122 of *Blish* are formed by depositing a single layer of metal within a trench and polishing back the metal using CMP (see column 5, lines 10-30), not using a plurality of stacked, interconnected, conductive layers as recited in claim 5. Also, in section 6, the Office Action indicates that FIG. 14 of *Blish* shows the sections protrude higher than the middle portion 104, and that column 2, lines 55-65 discloses

metal filled in the trench to form interconnect layer. However, middle portion 104 is a silicon layer (see column 4, line 30) not a conductive layer. Moreover, the *conductive layers* in *Blish* are not stacked. For at least these reasons, Applicant respectfully asserts that claim 5 is allowable over the cited reference.

With respect to claim 24, that claim recites:

> 24. A method of fabricating an integrated circuit seal ring comprising:
> providing an active area including semiconductor device structures; and
> forming a continuous conductive loop around the perimeter of said integrated circuit ***by forming and patterning a plurality of stacked, interconnected, conductive layers wherein said conductive loop has a plurality of sections having at least two different alternating widths*** wherein each of said different alternating widths has a different characteristic impedance, wherein said conductive loop forms said seal ring.

(*Emphasis Added*).

Applicant respectfully asserts that *Blish* is legally deficient for the purpose of anticipating claim 24, because at least the features/limitations emphasized above in claim 24 are not taught by *Blish*. For example, *Blish* does not teach forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers. Specifically, the sections 122 of *Blish* are formed by depositing a single layer of metal within a trench and polishing back the metal using CMP (see column 5, lines 10-30), not using a plurality of stacked, interconnected, conductive layers. Additionally, in section 6, the Office Action indicates that FIG. 14 of *Blish* shows the sections protrude higher than the middle portion 104, and that column 2, lines 55-65 discloses metal filled in the trench to form interconnect layer. However, middle portion 104 is a silicon layer (see column 4, line 30) not a conductive layer. Moreover, the *conductive layers* in *Blish* are not stacked. For at least these reasons, Applicant respectfully asserts that claim 24 is allowable over the cited reference.

Rejections under 35 U.S.C. 103

The Office Action indicates that claims 2-3, 6 - 7 and 25 - 26 stand rejected under 35 U.S.C. 103 as being rendered obvious by Blish et al. (U.S. 6,362,524). Applicant respectfully traverses the rejection. Specifically, Applicant respectfully asserts that the Offcie Action has not presented a prima facie case of anticipation for claims 1, 5, and 24 as set forth above. Since claims 2 and 3 are dependent claims that incorporate all the features/limitations of claim 1, claims 6-8 are dependent claims that incorporate all the features/limitations of claim 5, and claims 25 - 26 are dependent claims that incorporate all the features/limitations of claim 24, Applicant respectfully asserts that these claims also are in condition for allowance. In particular, the Office Action alleges no teaching or suggestion to remedy the deficiency of the respective rejections under 35 U.S.C. 102, therefore, Applicant respectfully requests that the rejections be removed and that these claims be placed in condition for allowance.

CONCLUSION

For the reasons as described above, Applicant respectfully asserts that the presently pending claims allowable over the cited references. Withdrawal of the rejections and allowance of the claims are respectfully requested. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Should Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone listed below.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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